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Frank Chau, Esq.
F. CHAU & ASSOCIATES, LLP
1900 Hempstead Turnpike, Suite 501
East Meadow, NY 11554

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,434	YOO ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/12/01 7/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending in the instant application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on June 12, 2001 and July 14, 2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

4. Claims 1-15 are objected to because of the following informalities:

Regarding claim 1, the claim contains terms which are lacking antecedent basis and may be considered to be indefinite. The following revised version of the claim is suggested by the Examiner:

A data recovery apparatus, comprising: a phase locked loop (PLL) for generating a plurality of phase clock signals each having a different delay time with respect to a clock signal;

an oversampler for M times oversampling serial input data in response to the plurality of phase clock signals and outputting a plurality of data bits in parallel;

a level transition detector for receiving the parallel data bits output from the oversampler, detecting ~~the~~ a point of time at which ~~the~~ a logic level transitions between

adjacent ones of the parallel data bits occurs and outputting the detection result as first through Mth transition signals;

a transition accumulator for accumulating the number of times each of the first through Mth transition signals is generated and outputting a one of a first through Mth transition accumulation signal associated with the one of the first through Mth transition signal whose generation frequency is ~~high~~ highest;

a state selector for generating a state signal in response to the one of the first through Mth transition accumulation signal output from the transition accumulator, wherein the state signal is used for selecting data bits of corresponding positions among the parallel data bits output from the oversampler; and

a data selector for receiving the parallel data bits, utilizing the state signal to select from the parallel data bits those data bits having sampling positions corresponding to the state of the state signal, and outputting the selected data bits in parallel.

Regarding claim 3, in line 8, the phrase "output the processing results as the first through third" should be replaced by –output a processing result as first through third--.

Regarding claim 4, in lines 4, 7, and 10, the phrase "input clock" is used although no antecedent basis for it definitely exists. The Applicant is requested to either provide antecedent basis for an *input* clock, or, alternatively, strike the word "input" thereby relying on the "a clock signal" (line 3, claim 1) as basis for "the clock signal". Further regarding claim 4, the use of "at a first level" in lines 4, 7, and 10 may cause an

indefinite interpretation of the claim. Specifically, "a first level" is defined three times and it is unclear if they are the same or different levels.

Regarding claim 6, the first and second bits of the state signal should be clearly defined to have logic states.

Regarding claim 10, in line 6, the phrase "outputting one" should be replaced by –outputting a one--, and, in line 8, the phrase "accumulating the number" should be replaced by –accumulating a number--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 10, 16, and 21 the use of the limitation "between adjacent" (i.e. claim 1, line 8; claim 10, line 5) is indefinite because the order of the parallel bits is not clearly related or defined. While the word adjacent is definitely interpreted as "next to", an order of the parallel bits is not clearly related to provide for a definite interpretation of which pair of bits should be chosen as adjacent to one another. As it is presently used in the claim, "adjacent bits" provides for an empty limitation due to the fact that the order of parallel bits is undefined. Therefore, a definitive interpretation of a particular pair of bits can not be made simply by claiming an adjacent one. To make the

claim definite, the Applicant is required to specify an ordering of the parallel bits in relation to something definite such as in a time order, for instance.

Regarding claim 5, taken in conjunction with parent claim 4, the claim is indefinite because the limitations of claims 4 and 5 are conflicting. In claim 4, the transition accumulator outputs one of a first, second, or third transition accumulation signal when a predetermined number of respective first, second or third transition signals are accumulated. However, in claim 5, which further limits claim 4 as a dependent claim, the transition accumulator outputs a transition signal rather than a first, second or third accumulation signal, and it is in response to a highest generation rather than an accumulation of a predetermined number. Therefore, the combination of the two claims is seemingly incongruent and indefinite.

Regarding claim 9, the claim is indefinite because a number of bits which are represented by 3P, 3P+1, and 3P+2 can not be clearly made. The claim should be amended to clearly define which bits are output under each respective circumstance of the state input signal. The definition of P should be made.

Regarding claims 13 and 18, the claims are indefinite because various interpretations of the word "initializing" in line 2 may be made. One is able to interpret initializing to mean "performing for the first time", "starting new", or "resetting". A definite interpretation may not be made.

Regarding claims 14 and 19, the claims are indefinite because the bit position which are represented by 3P, 3P+1, and 3P+2 can not be clearly made. The claims should be amended to clearly define which bits are output under each respective

circumstance of the detection of one of the transition signals in step (d). The definition of P should be made.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10-13, 15, 16, 17, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eglit (US 6272193).

Regarding claim 10, Eglit discloses (abstract; fig. 4) a data recovery method comprising the steps of receiving (via ADC 210, fig. 2) as input serial data (fig. 2, ref. 127) in blocks of K (K=20; col. 5, line 34) bits and performing an M times (M=3; col. 5, line 34) oversampling on each block of serial data using N (N=12; col. 5, lines 27-30 and line 33) phase clock signals having different delay times to output N data bits in parallel; detecting a transition in a level between adjacent ones of the N data bits (fig. 4, refs. 410 and 420; fig. 5; col. 9, lines 11-25; col. 10, lines 12-33) and outputting one of a first through Mth transition signals at the point of time of a detected level transition (col. 7, lines 47-68; col. 10, lines 27-33; col. 7, lines 33-39); accumulating (fig. 4, ref. 490) the number of generations of each of the first through Mth transition signals (col. 11, line 57-col. 12, line 35; *col. 12, lines 17-29*); detecting (fig. 5, ref. 495) the transition signal whose generation frequency has the greatest probability (col. 11, line 66-col. 12, line 5); and selecting (fig. 4, ref. 480) from the N data bits, K data bits corresponding to the

transition signal (col. 9, lines 45-57). Eglit does not disclose the detection of a transition signal whose generation frequency meets a predefined threshold exactly. However, Eglit discloses that the value of the static phase output or transition signal with the greatest frequency (fig. 4, ref. 495) is output according to a highest frequency or probability (col. 11, line 66-col. 12, line 5) which is hereby considered to be an obvious variation or interpretation of a predefined threshold because the predefined threshold is the threshold of having the greatest probability or frequency of occurrence.

Regarding claim 11, Eglit discloses the limitations of claim 10 as applied above. Further, as stated above, Eglit discloses that M is 3.

Regarding claim 12, Eglit discloses K is 20 and N is 12 as applied above in claim 10. Eglit does not disclose expressly that K is 4 as claimed in claim 12. However, at the time the invention was made, it would have been obvious to a one of ordinary skill in the art to receive data in any number of bits K per block and oversample them with any number of phases N. Applicant has not disclosed that the method of claim 11 wherein K is 4 provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with any number of bits per block K because the number of bits per block K simply determines how many bits are converted from serial to parallel simultaneously. One skilled in the art would clearly interpret the implications made by Eglit regarding the number of analog to digital converters (i.e. the values of K and N) that may be used (col. 5, lines 40-45) to create multiple various embodiments of the invention depending upon a desired balance between the number of bits per block K

to be converted (speed of serial to parallel conversion) and the amount of circuitry required to work on the K bits in parallel. Therefore, it would have been obvious to one of ordinary skill in this art to modify Eglit to obtain the invention as specified in claim 12.

Regarding claim 13, Eglit discloses the limitations of claim 11 as applied above. Further, Eglit discloses that the accumulation process is initialized or started upon the detection of a transition signal. It is inherent that the accumulation process is started when a transition signal is detected because the accumulation process performs the accumulations (i.e. it starts accumulating).

Regarding claim 15, Eglit discloses the limitations of claim 10 as applied above. Further, Eglit discloses that the step of selecting K data bits from the N data bits according to the detected transition signal comprises the generation of a state signal (fig. 4, ref. 458) comprising a predetermined value based on the detected transition signal in step (d) (fig. 4, ref. 495) and selecting (fig. 4, ref. 480) the N data bits based on the value of the state signal.

Regarding claim 16, Eglit discloses the limitations of the method steps (a)-(e) in the claim as applied to claim 10 above. Further, Eglit discloses that the method may be embodied as a program of instructions (commands) executable by a machine (CPU) to perform the method and stored on a storage device (RAM) readable by the machine (col. 15, lines 20-45).

Regarding claim 17, Eglit discloses the limitation of claim 16 as applied above. Further, Eglit discloses that M is 3 as applied to claim 16 above.

Regarding claim 18, Eglit discloses the limitations of claim 16 as applied above. Further, Eglit discloses that the accumulation process is initialized or started upon the detection of a transition signal. It is inherent that the accumulation process is started when a transition signal is detected because the accumulation process performs the accumulations (i.e. it starts accumulating).

Regarding claim 20, Eglit discloses the limitations of claim 16 as applied above. Further, Eglit discloses that the step of selecting K data bits from the N data bits according to the detected transition signal comprises the generation of a state signal (fig. 4, ref. 458) comprising a predetermined value based on the detected transition signal in step (d) (fig. 4, ref. 495) and selecting (fig. 4, ref. 480) the N data bits based on the value of the state signal.

Regarding claim 21, Eglit discloses the limitations of claim 21 as applied to claims 10 and 16 above.

9. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eglit in view of Lippman (US 3946379).

Regarding claim 1, Eglit discloses a data recovery apparatus, comprising: a phase locked loop (fig. 2, ref. 230) (PLL) for generating a plurality of phase clock signals each having a different delay time with respect to a clock signal (col. 5, lines 27-30); an oversampler (fig. 2, ref. 210) for M (M=3; col. 5, line 34) times oversampling serial input data in response to the plurality of phase clock signals and outputting a plurality of data bits in parallel (col. 5, lines 7-20; col. 25-35); a level transition detector (fig. 4, refs. 410 and 420; fig. 5; col. 9, lines 11-25; col. 10, lines 12-33) for receiving the parallel data bits

output from the oversampler, detecting the point of time at which the logic level transitions between adjacent ones of the parallel data bits and outputting the detection result as first through Mth transition signals (col. 7, lines 47-68; col. 10, lines 27-33; col. 7, lines 33-39); a transition accumulator (fig. 4, ref. 490) for accumulating the number of times each of the first through Mth transition signals is generated (col. 11, line 57-col. 12, line 35; *col. 12, lines 17-29*) and outputting a one of a first through Mth transition accumulation signal (fig. 5, ref. 495) or "static phase" associated with the transition signal whose generation frequency is high (col. 11, line 66-col. 12, line 5); a state selector (fig. 4, ref. 450) for generating a state signal (fig. 4, ref. 458) in response to the transition accumulation signal output from the transition accumulator, wherein the state signal is used for selecting data bits of corresponding positions among the parallel data bits output from the oversampler (col. 9, lines 18-24); and a data selector (fig. 4, ref. 480) for receiving the parallel data bits, utilizing the state signal (fig. 5, ref. 458) to select from the oversampled data bits having sampling positions corresponding to the state of the state signal, and outputting the selected data bit (col. 9, lines 45-57). In the disclosure of Eglit, the oversampling ratio M is equal to 3, and this relates to the three possible positions of a transition among the samples. The outputs of the oversampler (figs. 2 and 4, ref. 215) are bits communicated in parallel because, according to figure 5, the level transition detector requires the samples of the bits to be received in parallel to properly detect the occurrence of a transition at one of the 3 possible positions (early, neutral, or late). The transition accumulator or "score calculator" accumulates or keeps track of the number of times each of a particular transition position takes place. This

accumulation is performed to create a "static phase shift" or to create a probability that the transition has occurred at a particular position (col. 6, lines 44-55) over time. This static phase (fig. 4, ref. 495) is used as input to the state selector (fig. 4, ref. 450) for the appropriate selection of a chosen phase of the oversampled bit samples for output as the correct data (fig. 4, ref. 179). Eglit discloses oversampling (3 samples per bit) several data bits at once (col. 5, lines 33-35) and outputting, as selected data, one of the 3 samples of each of the oversampled data bits (col. 9, lines 45-53) but does not disclose that successive selected data bits are output in parallel. However, Lippman teaches a serial to parallel converter which appropriately samples serial data and outputs it in parallel by figure 1 (abstract). Further, Lippman teaches that many digital communications systems are designed to communicate serial data but devices such as computers and business machines handle data in groups of bits or in parallel (col. 1, lines 8-20). Thereby, Lippman teaches that a serial to parallel data converter can be used to interface a serial data communications stream with a machine to work with the data such as a computer. Therefore, it would have been obvious to one having ordinary skill in the art the time which the invention was made to output the serially input data stream of Eglit, which is already processed in parallel, in parallel form as taught by Lippman because, in such a state, the data would be immediately ready for processing by a computer or business machine.

Regarding claim 2, Eglit in view of Lippman disclose the limitations of claim 1 as applied above. Further, as stated above, Eglit discloses that M is 3.

Regarding claim 3, Eglit in view of Lippman disclose the limitations of claim 2 as applied above. Further, Eglit discloses by figure 5 that the level transition detector (fig. 4, refs. 410 and 420) comprises: a transition detector (fig. 4, ref. 410) comprising a plurality of exclusive OR gates (fig. 5) for performing an exclusive OR operation on two adjacent bits of the parallel data bits output from the oversampler and generating exclusive OR results as first, second, and third output signals (outputs of XOR gates); and a transition detection signal outputting unit (fig. 4, ref. 420) for processing the first, second, and third output signals to generate and output the processing results as the first through third transition signals (col. 9, lines 11-17; col. 10, lines 27-33).

Allowable Subject Matter

10. Indication of allowable subject matter is made regarding claim 4 if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 is indicated to contain allowable subject matter because the prior art of record does not disclose or make obvious a reset signal generator performing a logic combination on the first, second, and third transition accumulation signals and generating an accumulation reset signal for resetting the first, second, and third accumulators in response to the logic combination result.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art not relied upon above is cited to further show the state of the art with respect to serial to data converters.

U.S. Pat. No. 5313496 to de Geode.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
October 26, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER